ISSN:0975-9646

A Low Power Area Efficient Design for 1-bit Full Adder Cell

Manoj Kumar R and Krishna Murthy M

Department of ECE, MVGRCE, Andhra Pradesh, India

***Abstract*— In this paper we present a 1 bit Full Adder Cell. It was implemented with lesser number of transistors and lesser power consumption compared to the existing implementations of the Full Adder. Simulations are carried for supply voltages of 1.2v, 0.8v in HSPICE at 0.18µmCMOS technology. Proposed Full Adder results show that there was a reduction of power consumption and efficient in area. Area was measured using Micro Wind Tool.**

***Keywords*— Majority Function, Area , Power Consumption.**

I. INTRODUCTION

The demand and popularity of the portable electronics is driving the designers towards smaller silicon area, lesser power consumption and lesser delay. Full Adders are basic blocks of many circuits, especially in Arithmetic operations performed by processors, compressors, comparators, floating point unit and so on. There are many standard implementations in designing the Full Adder. Although the functionality is same, the way of producing the intermediate nodes and transistor count is varied. In different logic styles, one performance aspect is achieved at the cost of others. Small area and high performance are two conflicting constraints. The power consumed for any given function in CMOS circuit must be reduced for either of the two different reasons: One of these reasons is to reduce heat dissipation in order to allow a large density of functions to be incorporated on an IC chip. Any amount of power dissipation is worthwhile as long as it doesn't degrade overall circuit performance. The other reason is to save energy in battery operated instruments same as electronic watches where average power is in microwatts The logic style used basically influence the size, speed, wiring complexity and power dissipation. Circuit Size depends on the number of transistors, their sizes and on the wiring complexity.

In the second section various styles of Full Adder using Majority Function and the proposed Full Adder cell is implemented. In the third section simulation results, layout of the Proposed Full Adder is provided and comparison of power consumption for different power supply voltages and Area for different implementations are provided.

II. METHOD

Majority Function is a logic circuit which gives majority vote to determine the output. It is implemented using a buffer and three Capacitors. Capacitors output gives the majority function but with voltage levels $0,V_{dd}/3,2V_{dd}/3,V_{dd}$.To ensure only Low or High Logic levels a buffer is used([2],[4],[5]).These capacitors output acts as an input voltage for the Static Buffer to provide the majority function with Low or High Logic levels.

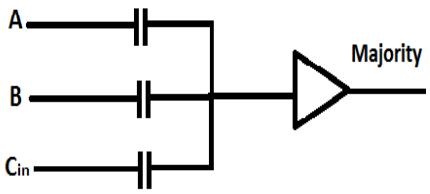

Fig.1 Majority Function

When majority of inputs are '0' then the output of the capacitor network considers it as either 0 or $V_{dd}/3$ and buffer considers it as logic 0 and gives output as Logic 0.

When majority of inputs are '1' then the output of the capacitor network considers it as either $2V_{dd}/3$ or V_{dd} and buffer considers it as logic 1 and gives output as logic 1 ([3],[6]-[9]).

TABLE I
VOLTAGE AT CAPACITOR'S OUTPUT AND OUTPUT OF THE BUFFER

A	B	C_{in}	o/p at Capacitors	Majority
0	0	0	0	0
0	0	1	$V_{dd}/3$	0
0	1	0	$V_{dd}/3$	0
0	1	1	$2V_{dd}/3$	1
1	0	0	$V_{dd}/3$	0
1	0	1	$2V_{dd}/3$	1
1	1	0	$2V_{dd}/3$	1
1	1	1	V_{dd}	1

A. The First Design

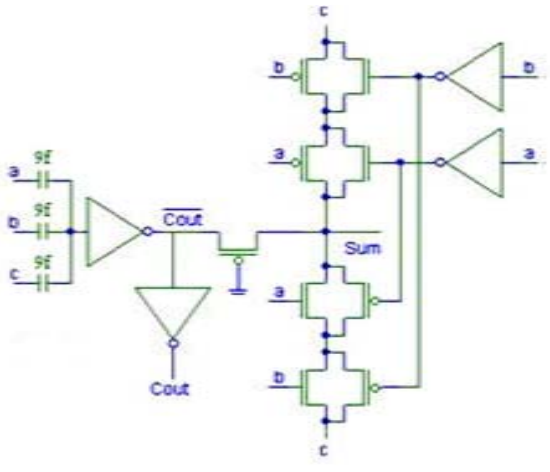

Fig.2 First Full Adder Cell

It is implemented using 17 transistors[1]. In this Sum is produced using Majority NOT function. Carry is directly taken from Majority Function.

B. The Second Design

It is implemented using 20 transistors. Output Carry is taken from the Majority structure. Sum is realized using NAND_NAND structure [1].

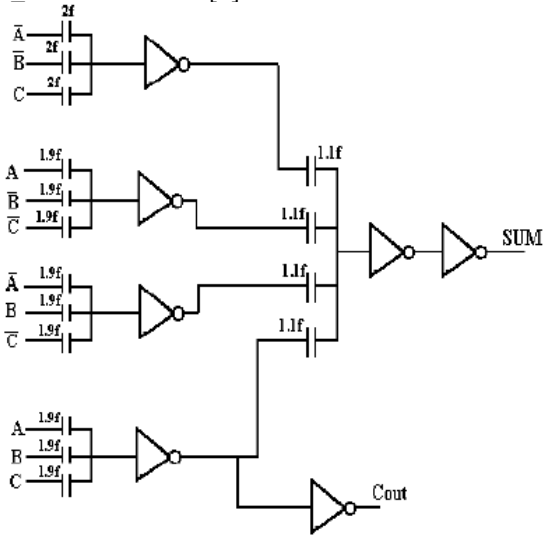

Fig.3 Second Full Adder Cell

C. Proposed Full Adder Cell

The New proposed Full Adder is implemented using 16 Transistors. The Functionality of a Full Adder based on Majority Function can be described as follows

$$Sum = A \oplus B \oplus C_{in}$$
$$= C_{out}(\Sigma(1,2,3,4,5,6)) + \overline{C_{out}}(\Sigma(0,7))$$

$$C_{out} = Maj(A, B, Cin) = AB + BC_{in} + C_{in}A$$

As C_{out} (Output Carry) and the majority function are same, C_{out} can be directly taken from majority function. Capacitors implement the Majority Structure. To enhance the voltage levels further two Inverters are used to get carry output.

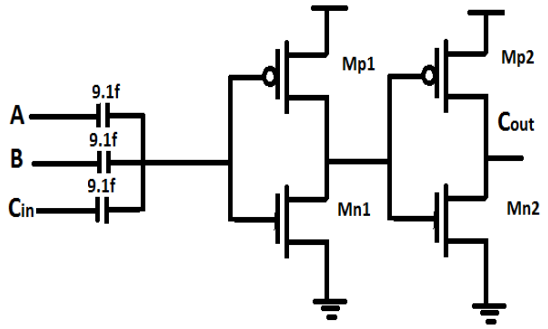

Fig.4 C_{out} using Majority Function and CMOS Inverter

For six Combinations i.e., from 001 to 110 $Sum=\overline{C_{out}}$. And for the remaining two combinations i.e., 000 and 111 Sum = C_{out} which can be shown in Table II.

So from C_{out} and $\overline{C_{out}}$, Sum can be obtained by giving both to the 2 X 1 Mux.

Now the selection line should be selected in such a way that for 001 to 110 C_{out} should be selected and for remaining two cases C_{out} should be selected.

So Sel should have one logic level for 000 and 111 while it should have opposite logic level for 001 to 110.Inorder to get such logic levels OR and NAND outputs should be multiplied i.e., ANDed.

TABLE II
TRUTH TABLE OF FULL ADDER

A	B	Cin	Cout	SUM	Majority Function
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	1	0
0	1	1	1	0	1
1	0	0	0	1	0
1	0	1	1	0	1
1	1	0	1	0	1
1	1	1	1	1	1

OR gate can be realized by first implementing the NOR using majority function followed by an Inverter and by changing the threshold values of Mp and Mn as shown in Fig 5 and Table III.

NAND gate can be also realized using Majority function by just changing the threshold values of the MOS transistors Mp and Mn as shown in Fig 5 and Table III.

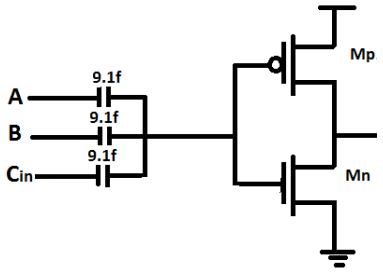

Fig.5 NOR and NAND using CMOS Inverter

TABLE III
IMPLEMENTING NOR AND NAND

A	B	Cin	NOR	NAND
0	0	0	Mp=ON, Mn=OFF	Mp=ON, Mn=OFF
0	0	1	Mp=OFF, Mn=ON	Mp=ON, Mn=OFF
0	1	0	Mp=OFF, Mn=ON	Mp=ON, Mn=OFF
0	1	1	Mp=OFF, Mn=ON	Mp=ON, Mn=OFF
1	0	0	Mp=OFF, Mn=ON	Mp=ON, Mn=OFF
1	0	1	Mp=OFF, Mn=ON	Mp=ON, Mn=OFF
1	1	0	Mp=OFF, Mn=ON	Mp=ON, Mn=OFF
1	1	1	Mp=OFF, Mn=ON	Mp=OFF, Mn=ON

In this Proposed Design, Three capacitors implement the majority function and followed by two inverters produce the Carry Output of Full Adder C_{out}. C_{out} and $\overline{C_{out}}$ are given to the multiplexer to select C_{out} for 000 and 111 combination while $\overline{C_{out}}$ for 001 to 110.

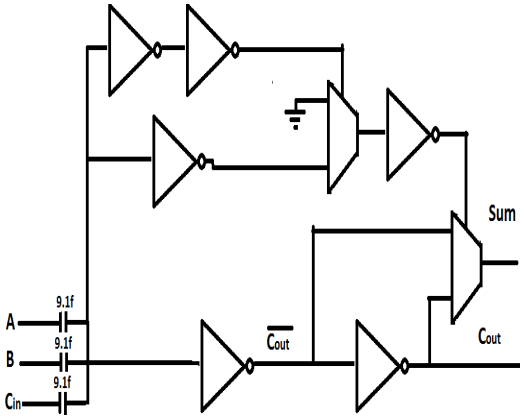

Fig.6 Proposed Full Adder Cell

The Selection line to the Mux is given by the OR and NAND outputs ANDed followed by an inverter.

New design is simulated at power supply voltage 1.2v and 0.8v.

III. RESULTS

The Proposed Full Adder Cell is simulated at0.18µm CMOS Process Technology using HSPICE.

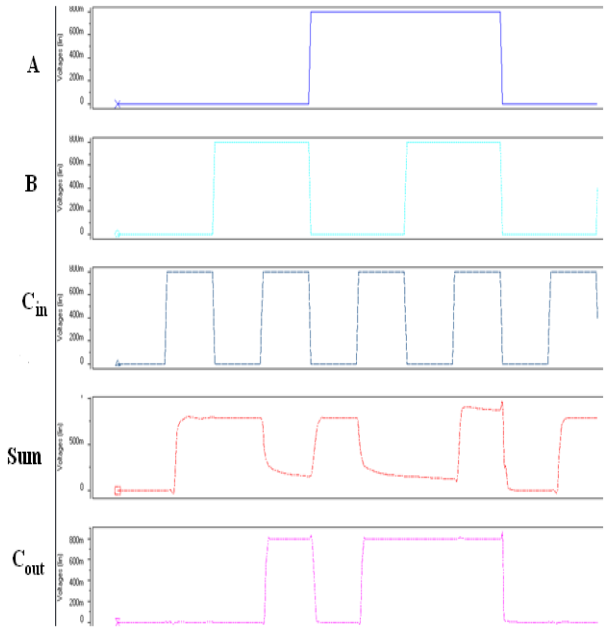

Fig.7 Waveforms of Proposed Full Adder (A, B, C_{in}, Sum, C_{out})

Average of Power consumption during all transitions gives the Power Consumption parameter. The Comparison of power consumptions with earlier designs is shown in table IV.

TABLE IV
POWER CONSUMPTION OF THE DESIGNS AT DIFFERENT SUPPLY VOLTAGES

	1.2v	0.8v
Designs	**Power(µw)**	**Power(µw)**
Design 1	4.5532	1.8724
Design 2	1.0545	0.5894
Proposed Full Adder Cell	0.66917	0.5179

The power consumption of new design is 0.66917(µw) which is 57.5% lower than Design 2 for 1.2v and is 0.5179(µw) which is lower than 13.8% Design2 for 0.8v.

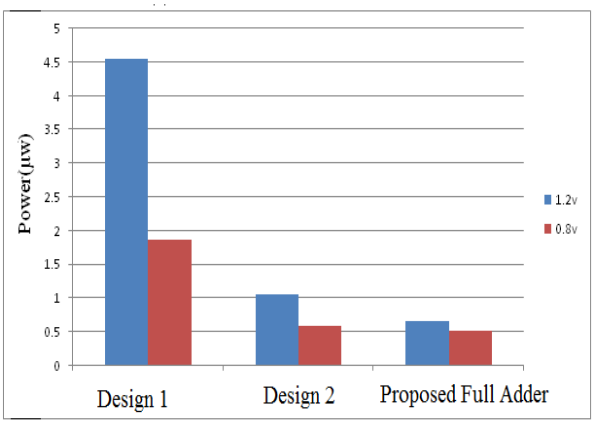

Fig.8 Comparison of Power Consumption for various Designs

The following is the layout of the Proposed Full Adder cell done in Microwind.

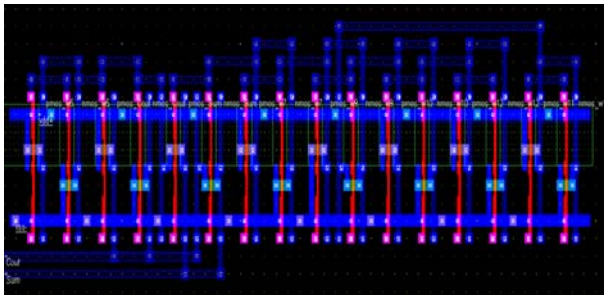

Fig.9 Layout of Proposed Full Adder

Area of Proposed design is compared with the earlier designs in Fig .10.It was measured using Microwind Tool.

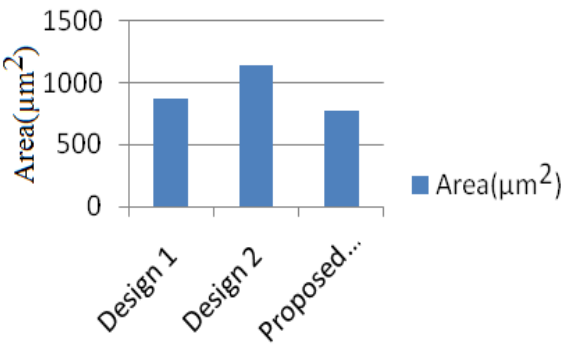

Fig.10 Comparison of Area for different Designs

IV. CONCLUSION

A New Full Adder cell has been presented which is simulated at 0.18µm CMOS Technology using HSPICE at different supply voltages which showed significant improvement in power consumption compared to earlier designs. Area was also very efficient.

REFERENCES

[1] K.Navi, H.Mokari, G.Zandkarimi, "A New Low Power CMOS Full Adder", IEEE Conferences, 2010.

[2] Ashkan Khatir , Shaghayegh Abdolahzadegan ,Iman Mahmoudi, "High Speed Multiple Valued Logic Full Adder Using CArbon Nano Tube Field Effect Transistor", International Journal of VLSI design & Communication Systems (VLSICS) Vol.2, No., 2011.

[3] K. Navi, R. Faghih Mirzaee, M. H. Moaiyeri, B. Mazloom Nezhad, O. Hashemipour, K. Shams, "Ultra high speed Full Adders", IEICE Electronics Express, vol.5, no.18 .

[4] Omid Daei, Keivan Navi, Mohammad Reza Saatchi, "AHigh-Speed Hybrid Full Adder" European Journal of Scientific Research, Vol.26 No.1, 2009.

[5] Keivan Navi, Mehrdad Maee, Vahid Foroutan, Somayeh Timarchi, Omid Kavehe,"A novel low-power full-adder cell for low voltage", INTEGRATION, VLSI Journal.

[6] Neda Khandel, Kevin Navi, "The Design of a High-Performance Full Adder cell by combining common digital gates and Majority Function",European Journal of Scinetific Research,Vol.23 No.4, 2008.

[7] Subodh Wairya, Rajendra Kumar Nagaria, and Sudarshan Tiwari, "Performance Analysis of High Speed Hybrid CMOS Full Adder Circuits for Low Voltage VLSI Design".

[8] Vahid Foroutan, Keivan Navi and Majid Haghparast, "A New Low Power Dynamic Full Adder Cell Based on Majority Function", World Applied Sciences Journal 4 (1): 133-141, 2008.

[9] C.H.Chang, M.Zhang and J.Gu, "A Novel low power low voltage full adder cell", 3rd International Symposium on Image and Signal Processing and Analysis, Vol.1, 2003.